Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. CP0**
2. **Q1**
3. **P1**
4. **P3**
5. **Q3**
6. **N. MR**
7. **VCC**
8. **N. PL**
9. **Q2**
10. **P2**
11. **P0**
12. **Q0**
13. **N. CP1**
14. **GND**

**.066”**

**4 3**

**5**

**6**

**7**

**8**

**9**

**2**

**1**

**14**

**13**

**12**

**10 11**

**MASK**

**REF**

**LS197**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref: LS197**

**APPROVED BY: DK DIE SIZE .055” X .066” DATE: 8/8/23**

**MFG: MOTOROLA THICKNESS .020” P/N: 54LS197**

**DG 10.1.2**

#### Rev B, 7/1